In the Claims:

1. (Previously Presented) An integrated circuit arrangement,

having an electrically insulating insulating region, and

having at least one sequence of regions which forms a capacitor and which contains, in the order specified:

an electrode region near the insulating region,

a dielectric region, and

an electrode region remote from the insulating region, the insulating region being part of an insulating layer arranged in a plane,

the capacitor and at least one active component of the integrated circuit arrangement being arranged on the same side of the insulating layer, and the electrode region near the insulating region and an active region of the component being arranged in a plane which lies parallel to the plane in which the insulating layer is arranged,

wherein the electrode region near the insulating region is a monocrystalline region containing a multiplicity of webs, or

at least one field-effect transistor is present in which:

a channel region is the active region,

the field-effect transistor contains at least one web,

a plurality of control electrodes is arranged at mutually opposite sides of the web,

a connecting region electrically connects the control electrodes, the connecting region is isolated from the channel region by a thick insulating region, the thick insulating region has an insulating thickness which is greater than a thickness of control electrode insulation regions, and

the control electrodes contain the same material as the electrode region remote from the insulating region.

2. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein at least one of:

the electrode region near the insulating region is a monocrystalline region,

at least one of the electrode region near the insulating region or the active region has a thickness of less than one hundred nanometers,

the active region is a monocrystalline region,

the insulating layer adjoins, at one side, a carrier substrate,

the insulating layer adjoins the electrode region near the insulating region at an opposing side,

boundary areas lie completely in two mutually parallel planes,

the insulating layer comprises an electrically insulating material, or

the active component is a transistor.

3. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein at least one of:

the dielectric region comprises silicon dioxide,

the dielectric region comprises a material having a dielectric constant of greater than four,

the electrode region remote from the insulating region comprises silicon,

the electrode region remote from the insulating region comprises a metal,

the electrode region remote from the insulating region contains a low-impedance material, or

the electrode region remote from the insulating region adjoins a region containing metal-semiconductor compounds.

4. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein at least one of:

the dielectric region and the electrode region remote from the insulating region are arranged at at least two side areas of the electrode region near the insulating region, or

the electrode region near the insulating region contains a multiplicity of webs whose web height is larger than a web width.

5. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein the at least one field-effect transistor further contains at least one of:

a control electrode that contains material of the same dopant concentration as the electrode region remote from the insulating region,

a control electrode insulation region that contains at least one of the same material or a material having the same thickness as that of the dielectric region, or

a control electrode insulation region that contains at least one of a different material or a material having a different thickness than the dielectric region.

6. (Previously Presented) The circuit arrangement as claimed in claim 5, wherein at least one of:

at least one control electrode adjoins a region containing metal-semiconductor compounds, or

the connecting region at least one of: comprises the same material or has the same doping level as the electrode region remote from the insulating region.

7. (Previously Presented) The circuit arrangement as claimed in claim 5, wherein at least one of:

one terminal region or both terminal regions of the field-effect transistor adjoin the insulating layer,

at least one terminal region of the field-effect transistor adjoins a region containing a metal-semiconductor compound, or

the terminal regions of the field-effect transistor have a larger thickness than the active region.

8. (Previously Presented) The circuit arrangement as claimed in claim 5, wherein at least one of:

spacers are arranged on both sides of the control electrodes, which comprise a different material than the electrode layer,

a spacer is arranged at at least one side of the electrode region remote from the insulating region, which comprises a different material than the electrode layer, or

a spacer arranged at a control electrode and a spacer arranged at the electrode region remote from the insulating region touch one another.

9. (Previously Presented) The circuit arrangement as claimed in claim 5, wherein at least one of:

a terminal region of the field-effect transistor and the electrode region of the capacitor which is near the insulating region adjoin one another and have an electrically conductive connection at a boundary,

the terminal region of the field-effect transistor which adjoins the electrode region does not adjoin a region containing a metal-semiconductor compound, or

another terminal region of the field-effect transistor adjoins a region containing a metal-semiconductor compound.

10. (Previously Presented) The circuit arrangement as claimed in claim 9, wherein a side of the electrode region near the insulating region which adjoins the terminal region is longer than a side of the electrode region near the insulating region which lies transversely with respect to the side which adjoins the terminal region, the transistor has a transistor width which is a multiple of a minimum feature size, or

the side of the electrode region near the insulating region which lies transversely with respect to that side of the electrode region near the insulating region which adjoins the terminal region is longer than the side adjoining the terminal region, the transistor has a transistor width which is less than three times the minimum feature size.

11. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein at least one of:

the circuit arrangement contains at least one processor,

the capacitor and the active component form a memory cell, or

the memory cell contains either a capacitor and only one transistor or a capacitor and more than one transistor.

12. (Previously Presented) A method for fabricating an integrated circuit arrangement with a capacitor,

in which the following method steps are performed without any restriction by the order specified:

providing a substrate containing an insulating layer made of electrically insulating material and a semiconductor layer, the insulating layer containing an insulating region,

patterning the semiconductor layer in order to form at least one electrode region for a capacitor and in order to form at least one active region for a transistor,

after the patterning of the semiconductor layer, producing at least one dielectric layer,

after the production of the dielectric layer producing an electrode layer,

forming an electrode of the capacitor which is remote from the insulating region in the electrode layer,

forming a control electrode of the transistor taking place at the same time as the formation of the electrode region remote from the insulating region, and

either:

an electrode region near the insulating region containing a multiplicity of webs, or

the transistor being a field-effect transistor, a channel region of which is the active region, the field-effect transistor containing at least one web, a plurality of control electrodes arranged at mutually opposite sides of the web, a connecting region electrically connecting the control electrodes, the connecting region isolated from the channel region by a thick insulating region, the thick insulating region has an insulating thickness which is greater than a thickness of control electrode insulation regions.

13. (Previously Presented) The method as claimed in claim 12, further comprising:

applying at least one insulating layer to the semiconductor layer prior to patterning,

doping the electrode near the insulating region, , or

producing the dielectric layer at the same time as a dielectric layer at the active region of the transistor.

14. (Previously Presented) The method as claimed in claim 12 further comprising at least one of:

producing an auxiliary layer after the production of the electrode layer, or

patterning at least one of an electrode region remote from the insulating region or a control electrode of the transistor using the auxiliary layer as a hard mask.

15. (Previously Presented) The method as claimed in claim 12, further comprising at least one of:

applying a further auxiliary layer after the patterning of a control electrode of the transistor or

anisotropically etching the further auxiliary layer.

16. (Previously Presented) The method as claimed in claim 12, further comprising at least one of:

repeatedly patterning the insulating layer, a thickness of an auxiliary layer being reduced, or

anisotropic etching a further auxiliary layer after the patterning the insulating layer.

17. (Previously Presented) The method as claimed in claim 12, further comprising at least one of:

carrying out a selective epitaxy on uncovered regions made of semiconductor material after at least one of the formation of an electrode region remote from the insulating region or the patterning of a control electrode of the transistor, or

doping terminal regions of the transistor after at least one of the formation of the electrode region remote from the insulating region or after the patterning of the control electrode.

18. (Previously Presented) The method as claimed in claim 12, further comprising at least one of:

removing an auxiliary layer, after at least one of the patterning of the insulating layer (or after the carrying out of selective epitaxy, or

selectively forming a metal-semiconductor compound on at least one of the electrode layer or on uncovered semiconductor regions.